# CLAIMS

What is claimed is:

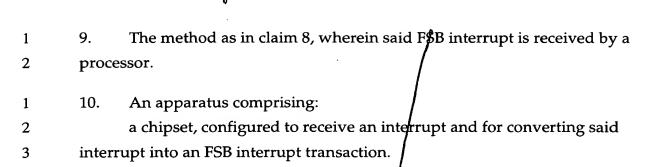1. A method comprising:

receiving an interrupt;

converting said interrupt into an upstream memory write interrupt; and

converting said upstream memory write interrupt into a front side bus
(FSB) interrupt transaction.

2. The method as in claim 1, wherein said interrupt is generated by a
peripheral component interconnect (PCI) device.

3. The method as in claim 2, wherein said FSB interrupt is received by a
processor.

4. A method comprising:

receiving a message signaled interrupt (MSI) interrupt;

forwarding said MSI interrupt; and

converting said MSI interrupt into an FSB interrupt transaction.

5. The method as in claim 4, wherein said MSI interrupt is generated by a
PCI device, and wherein said FSB interrupt is received by a processor.

6. The method as in claim 5, wherein said FSB interrupt is received by a
processor.

7. A method comprising:

receiving a hardware signal;

converting said hardware signal into an upstream memory write
interrupt; and

converting said upstream memory write interrupt into an FSB interrupt
transaction.

8. The method as in claim 7, wherein said hardware signal is generated by a
PCI device, and wherein said FSB interrupt is received by a processor.

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1     9.     The method as in claim 8, wherein said FSB interrupt is received by a
2     processor.

1     10.     An apparatus comprising:
2         a chipset, configured to receive an interrupt and for converting said
3     interrupt into an FSB interrupt transaction.

1     11.     The apparatus as in claim 10, said chipset further comprising at least one
2     of an I/O controller hub (ICH), P64H, AGP device.

1     12.     The apparatus as in claim 11, further comprising an I/O component of an
2     advanced programmable interrupt controller (IOxAPIC) configured to convert
3     said interrupt into an upstream memory write interrupt.

1     13.     The apparatus as in claim 12, said chipset further comprising a HUB
2     interface coupled on a first end to said IOxAPIC and coupled on a second end to
3     a MCH, wherein said memory controller hub (MCH) configured to convert said
4     upstream memory write interrupt into a FSB interrupt transaction.

1     14.     The apparatus as in claim 10, wherein said interrupt is generated by a PCI
2     device, and wherein said chipset is coupled to a processor.

1     15.     The apparatus as in claim 10, wherein said interrupt is a MSI interrupt.

1     16.     The apparatus as in claim 15, said chipset further comprising a HUB
2     interface coupled on a first end to an ICH and coupled on a second end to a
3     MCH, wherein said ICH configured to forward said MSI interrupt to said HUB
4     interface, and wherein said MCH configured to convert said MSI interrupt into a
5     FSB interrupt transaction.

1     17.     The apparatus as in claim 16, wherein said MCH configured to ensure at
2     least one data pipe of a HUB interface is flushed upstream before propagating an
3     interrupt upstream.

1     18.     The apparatus as in claim 16, wherein said MCH configured to receive an
2     end of interrupt (EOI) from a processor and broadcast said EOI to at least one

3   downstream HUB interface IOxAPIC generating at least one level mode
4   ~~interrupt.~~

1   19.    An apparatus comprising:
2          an MCH configured to redirect at least one interrupt based on task priority
3   information.

1   20.    The apparatus as in claim 19, wherein said task priority information is
2   downloaded by a processor into said MCH having a task priority register (TPR)
3   and FSB XTPR update transactions.

1   21.    The apparatus as in claim 19, wherein said interrupt is an upstream
2   memory write interrupt.

1   22.    The apparatus as in claim 19, wherein said interrupt is an IPI interrupt.

1   23.    The apparatus as in claim 19, wherein said interrupt is marked as lowest
2   priority re-directable, and redirected to a lowest priority register.

1   24.    A method comprising
2          redirecting at least one interrupt based on task priority information.

1   25.    The method as in claim 24, wherein said interrupt is an upstream memory
2   write interrupt.

1   26.    The method as in claim 24, wherein said interrupt is an IPI interrupt.

1   27.    The method as in claim 24, wherein said interrupt is marked as lowest
2   priority re-directable, and redirected to a lowest priority register.

1   28.    A method comprising:
2          providing preferred ordering of at least one XTPR update transaction and
3   at least one interrupt to be redirected.

1   29.    The method as in claim 28, further comprising ensuring valid information
2   is used for an interrupt redirection when an XTPR update transaction and an
3   interrupt occur about the same time.

1   30.    The method as in claim 29, further comprising providing support for said
2   XTPR update transactions to update at least one XTPR register.